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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/819,626	03/29/2001	Andrew M. Lever	M4065.0432/P432	4425
24998	7590	03/05/2004	EXAMINER	
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP			NGUYEN, LINH M	
2101 L STREET NW			ART UNIT	
WASHINGTON, DC 20037-1526			PAPER NUMBER	

2816

DATE MAILED: 03/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	<b>Application No.</b> 09/819,626	<b>Applicant(s)</b> LEVER, ANDREW M.	
	<b>Examiner</b> Linh M. Nguyen	<b>Art Unit</b> 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12/16/20003 and 01/06/2004.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-4,8 and 23-29 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4,8 and 23-29 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 March 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

This is a response to the Applicant's amendment submitted on 12/16/2003. According to this amendment, claims 5-7 and 9-22 are canceled; thus, claims 1-4, 8, and 23-29 are now presented in the instant application.

#### **RCE acknowledgement/ Prosecution reopened**

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114.

Applicant's submission filed on 01/06/2004 has been entered.

#### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

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3. Claims 1-4, 8, and 23-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Ingino, Jr. (U.S. Patent No. 6,441,660).

With respect to claims 1 and 23, Ingino Jr. discloses, in Figs. 1 and 3, and col. 8, lines 7-16, a charge pump circuit and a corresponding operating method comprising *(from here on transistors in reference numerals [40] and [42] will be designated with similar reference numeral as [M<sub>s1</sub>, M<sub>d2</sub>, and M<sub>c1</sub>,] and [M<sub>c2</sub>, M<sub>d3</sub>, and M<sub>s2</sub>] with “ ’ (prime) ” notation for distinction)* (1) a first plurality of serially connected transistors [M<sub>s1</sub>’, M<sub>c1</sub>’] of a first conductivity type, and (2) a second plurality of serially connected transistors [M<sub>c2</sub>’, M<sub>s2</sub>’] of a second conductivity type; wherein (i) the first plurality of serially connected transistors are serially connected to the second plurality of serially connected transistors, (ii) the interconnection of the first and second plurality of transistors provides an output [V<sub>dummy</sub>] to be coupled to a load device *(circuit with output [V<sub>dummy</sub>] is similar to circuit with V<sub>ctrl</sub> output (col. 8, lines 7-17); therefore, V<sub>dummy</sub> could be connected similarly to a load circuit (i.e. loop filter, VCO) as V<sub>ctrl</sub> (Fig. 1)*, (iii) a gate of one of the first plurality of transistors [M<sub>s1</sub>’] for receiving a DOWN\ pulse signal [Down\], (iv) a gate of another one of the first plurality of transistors [M<sub>c1</sub>’] for receiving a DC bias signal, (v) a gate of one of the second plurality of transistors [M<sub>s2</sub>’] for receiving an UP pulse signal [Up], (vi) a gate of the other of the second plurality of transistors [M<sub>c2</sub>’] for receiving another DC bias signal, (vii) a first node [at M<sub>d2</sub>’] at the interconnection of the transistors of the first plurality of transistors for receiving a DOWN pulse signal [Down], and (viii) a second node [at M<sub>d3</sub>’] at the interconnection of the transistors of the second plurality of transistors for receiving an UP\ pulse signal [Up\].

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With respect to claim 2, Ingino Jr. discloses, in Fig. 3 and col. 7, lines 9-14, that the first plurality of transistors  $[M_{s1}', M_{c1}']$  are p-channel transistors, and that the second plurality of transistors  $[M_{c2}', M_{s2}']$  are n-channel transistors.

With respect to claims 3 and 24, Fig. 3 of Ingino Jr. further discloses a first capacitor circuit  $[M_{d2}']$  for coupling the DOWN pulse signal to the first node and a second capacitor circuit  $[M_{d3}']$  for coupling the UP pulse signal to the second node.

With respect to claim 4, Figs. 1 and 3 of Ingino Jr. discloses that the first plurality of transistors  $[M_{s1}', M_{c1}']$  include a pair of transistors, and the second plurality of transistors  $[M_{c2}', M_{s2}']$  include a pair of transistors.

With respect to claim 8, Figs. 1 and 3 of Ingino Jr. discloses a charge pump circuit comprising (1) a first plurality of serially connected transistors  $[M_{s1}', M_{c1}']$  of a first conductivity type [p-channel transistors], and (2) a second plurality of serially connected transistors  $[M_{c2}', M_{s2}']$  of a second conductivity type [n-channel transistors]; wherein (i) the first plurality of serially connected transistors are serially connected to the second plurality of serially connected transistors, (ii) the interconnection of the first and second plurality of transistors provides an output  $[V_{dummy}]$  for being coupled to a load device (*circuit with output  $[V_{dummy}]$  is similar to circuit with  $V_{ctrl}$  output (col. 8, lines 7-17); therefore,  $V_{dummy}$  could be connected similarly to a load circuit (i.e. loop filter, VCO) as  $V_{ctrl}$  (Fig. 1)*), (iii) a gate of one of the first plurality of transistors  $[M_{s1}']$  for receiving a first switching signal [Down], (iv) a gate of another one of the first plurality of transistors  $[M_{c1}']$  for receiving a DC bias signal, (v) a gate of one of the second plurality of transistors  $[M_{s2}']$  for receiving a second switching signal [Up], (vi) a gate of the other of the second plurality of transistors  $[M_{c2}']$  for receiving another DC bias signal,

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(vii) a first node [at  $M_{d2}$ ] at the interconnection of the transistors of the first plurality of transistors for receiving a complementary first switching signal [Down], and (viii) a second node [at  $M_{d3}$ ] at the interconnection of the transistors of the second plurality of transistors for receiving a complementary second switching signal [Up\].

With respect to claim 25, Fig. 1 of Ingino Jr. discloses that load device comprises a filter [28] *(as indicated in the above paragraph, circuit with output  $V_{dummy}$  is similar to circuit with  $V_{ctrl}$  output (col. 8, lines 7-17); therefore,  $V_{dummy}$  could be connected similarly to a load circuit (i.e. loop filter, VCO) as  $V_{ctrl}$  (Fig. 1).*

With respect to claim 26, Fig. 1 of Ingino Jr. discloses that the load device comprises an input of a voltage controlled oscillator [VCO, 20] *(as indicated in the above paragraph, circuit with output  $V_{dummy}$  is similar to circuit with  $V_{ctrl}$  output (col. 8, lines 7-17); therefore,  $V_{dummy}$  could be connected similarly to a load circuit (i.e. loop filter, VCO) as  $V_{ctrl}$  (Fig. 1).*

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ingino, Jr. in view of Applicant Admitted Prior Art (Fig. 1).

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With respect to claim 27, Ingino, Jr. discloses all of the claimed subject matter, as expressly recited in claim 1, except for the Down pulse signal being received directly from a phase frequency detector.

Applicant Admitted Prior Art (Fig. 1) discloses a charge pump circuit [11] directly receiving a DOWN signal from a phase detector circuit [13].

To feed a DOWN pulse signal directly into the first node of Ingino's charge pump circuit to reduce transmitting or propagating noise resulted from additional device(s) along the signal path would have been obvious to one of ordinary skill in the art at the time of the invention since such configuration with direct connection for transmitting noise reduction has been a well-known practice as evidenced by the teachings of Applicant Admitted Prior Art (Fig. 1).

With respect to claim 28, Ingino, Jr. discloses all of the claimed subject matter, as expressly recited in claim 8, except for the first switching signal being received directly from a phase frequency detector.

Applicant Admitted Prior Art (Fig. 1) discloses a charge pump circuit [11] directly receiving a switching signal (i.e. DOWN, UP) from a phase detector circuit [13].

To feed a switching signal directly into the first node of Ingino's charge pump circuit to reduce transmitting or propagating noise resulted from additional device(s) along the signal path would have been obvious to one of ordinary skill in the art at the time of the invention since such configuration with direct connection for transmitting noise reduction has been a well-known practice as evidenced by the teachings of Applicant Admitted Prior Art (Fig. 1).

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With respect to claim 29, Ingino, Jr. discloses all of the claimed subject matter, as expressly recited in claim 23, except for the first applied switching signal being received directly from a phase frequency detector.

Applicant Admitted Prior Art (Fig. 1) discloses a charge pump circuit [11] directly receiving a switching signal (*or first applied switching signal*) (i.e. DOWN, UP) from a phase detector circuit [13].

To feed a switching signal (*or first applied switching signal*) directly into the first node of Ingino's charge pump circuit to reduce transmitting or propagating noise resulted from additional device(s) along the signal path would have been obvious to one of ordinary skill in the art at the time of the invention since such configuration with direct connection for transmitting noise reduction has been a well-known practice as evidenced by the teachings of Applicant Admitted Prior Art (Fig. 1).

### ***Remarks and Conclusion***

5. Applicant's arguments filed 12/16/2004 have been fully considered but they are not persuasive.

With respect to the Applicant's argument on amended claim 1, at page 8, first paragraph, line1- 2, the Examiner disagrees with the Applicant's statement that "*Indigo does not teach that  $V_{dummy}$  is an output adapted to be coupled to a load device*". As shown in col. 8, lines 7-16, Ingino, Jr. discloses a circuit on the right side having  $V_{dummy}$  is similar to the circuit on the left side with output  $V_{ctrl}$  (col. 8, lines 7-16). One skills in the art would see that with similar structure,  $V_{dummy}$  would be the output for the right side circuit and could be connected similarly to a load circuit (i.e. loop filter, VCO) as  $V_{ctrl}$  (Fig. 1). Furthermore, this language is merely for



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intended use and one skills in the art would see that  $V_{dummy}$  is capable of being coupled to a load circuit. Hence, claim 1 remains rejected under 35 USC 102 claim rejections.

With respect to the Applicant's argument on amended claim 8, at page 8, fourth paragraph, lines 1-5, as similarly discussed above, the Examiner disagrees with the Applicant's indication that Indigo does not teach or suggest "an output, said output being adapted to be coupled to a load device.". As indicated in the above paragraph,  $V_{dummy}$  is the output for the right side circuit since the circuit on the right side having  $V_{dummy}$  similar to the circuit on the left side with output  $V_{ctrl}$  and thus one skills in the art would know that  $V_{dummy}$  could be connected similarly to a load circuit (*i.e. loop filter, VCO*) as  $V_{ctrl}$  (Fig. 1). Furthermore, this language is merely for intended use and one skills in the art would see that  $V_{dummy}$  is capable of being coupled to a load circuit.

With respect to the Applicant's argument on amended claim 23, at page 9, first paragraph, lines 3-4, the Examiner disagrees with the Applicant's statement that "*the Indigo reference does not teach or suggest "an output terminal ...between said bias transistors"*". As clearly shown, in Fig. 3 of Indigo et al., a circuit and its corresponding method of operating a charge pump comprising: switching a first switching transistor in response to a first applied switching signal to affect an output at an output terminal adapted to be coupled to a load device. Similarly, as indicated above,  $V_{dummy}$  is the output for the right side circuit since the circuit on the right side having  $V_{dummy}$  similar to the circuit on the left side with output  $V_{ctrl}$  and thus one skills in the art would know that  $V_{dummy}$  could be connected similarly to a load circuit (*i.e. loop filter, VCO*) as  $V_{ctrl}$  (Fig. 1). Furthermore, this language is merely for intended use and one skills in the art would see that  $V_{dummy}$  is capable of being coupled to a load circuit.

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Rejections on claims 2-4 and 25-26 remain since each depend directly from claim 1, rejections on claim 28 remain since claim 28 depends directly from claim 8, and rejections on claims 24 and 29 remain since each depends directly from claim 23.

***Inquiry***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linh M. Nguyen  
Examiner  
Art Unit 2816

LMN

A handwritten signature in black ink, appearing to read 'Linh M. Nguyen', with a long horizontal flourish extending to the right.